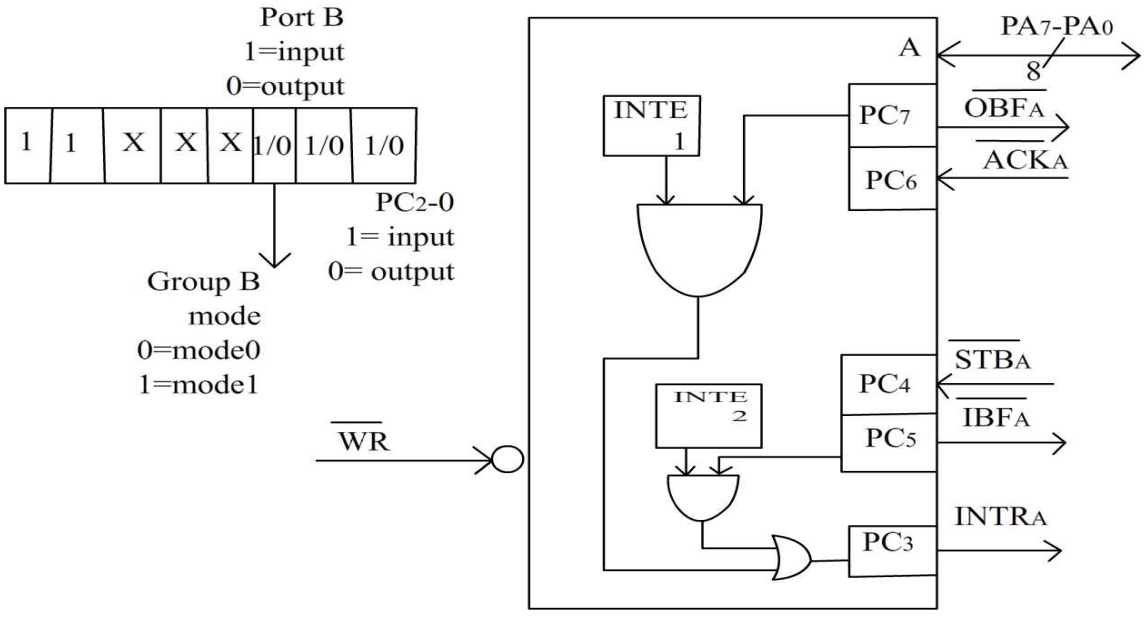
Lecture-45

Mode 2: (Strobed Bidirectional bus I/O)

This functional configuration provides means for communicating with a peripheral device on a single 8-bit data bus for both transmitting and receiving data control and status lines (hg and shake signal) are provided to handily the flows of data on the I/O bus. Interrupt generation and enable/ disable functions are also available. The mode2 functional definitions are as follows:

1. Used by Group A only/
2. An 8-bit bidirectional I/O port (PORT B) and a 5-bit control port (PORTC).
3. Both input & outputs are latched.
4. The 5-bits of PORT C are used for control and status of PORT A.
5. PORT B is available for either mode 0 or mode 1 operation.

Fig shows an 8255 set up with PORT A on mode 2,



Control signal definitions:

The functions of PORT C as determined by mode 2 are shown below.

OUTPUT operation

PC_7: $\overline{OBFA}$ output buffer full PORT A.

The $\overline{OBF}$ output will go low to indicate that the CPU has written data out to specified port. The $\overline{OBFA}^{lim}$ will be set by the rising edge of $\overline{WR}$ input and reset by $\overline{ACKA}$ input being low.

PC_7: $\overline{ACKA}$ Acknowledge port A

A low on this input informs the 8255, the data from port A has been accepted. The difference between $\overline{ACKA}$ in mode 1& mode 2 is that in mode 2 the output of the PORT A is normally in a tri-state condition, so the $\overline{ACKA}$ signal enables the output buffer of PORT A in addition to indicating that the external device has accepted the PORT A data.

INTE F/F 1:

The interrupt enable INTE f/f associated with OBF. It is controlled by bit set/reset of PC_6.

Input operation:

PC_4: $\overline{STBA}$

Input strobe for PORT A. A low on this input loads data into the input latch.

PC_5: IBFA

Input is full PORT A. A high in this output indicate that data has been loaded into the input latch.

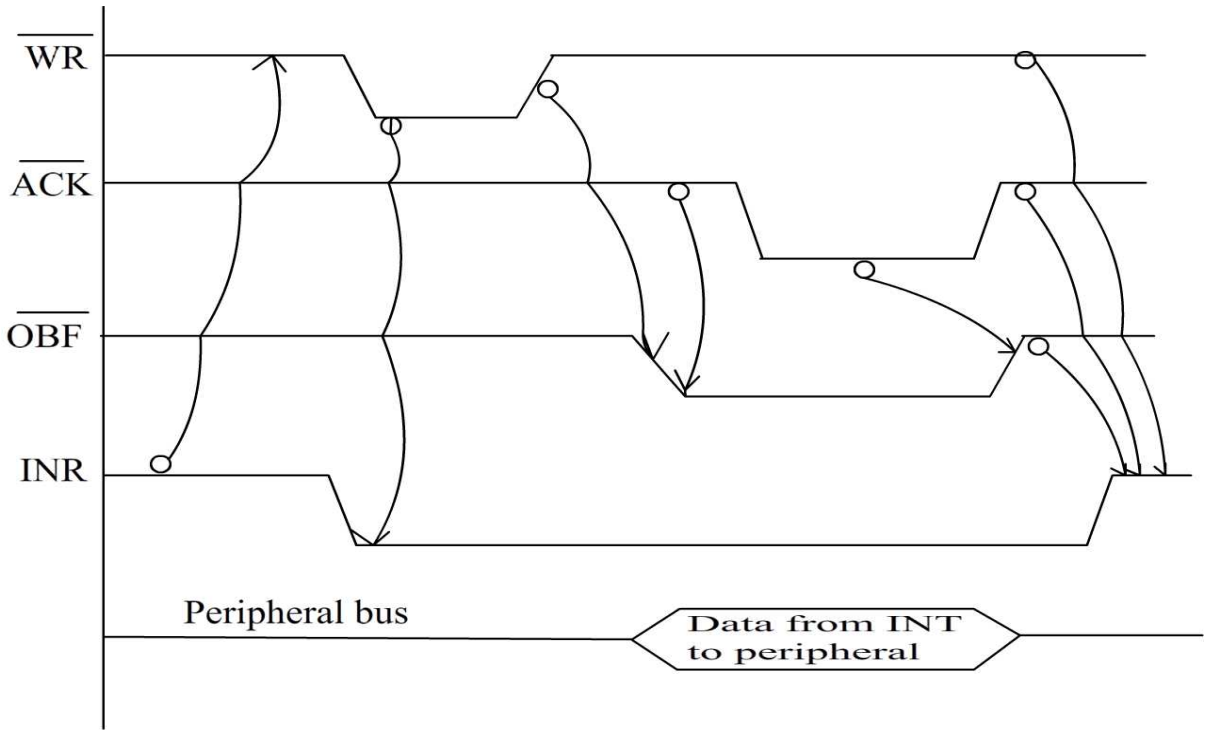
INTEL 2:

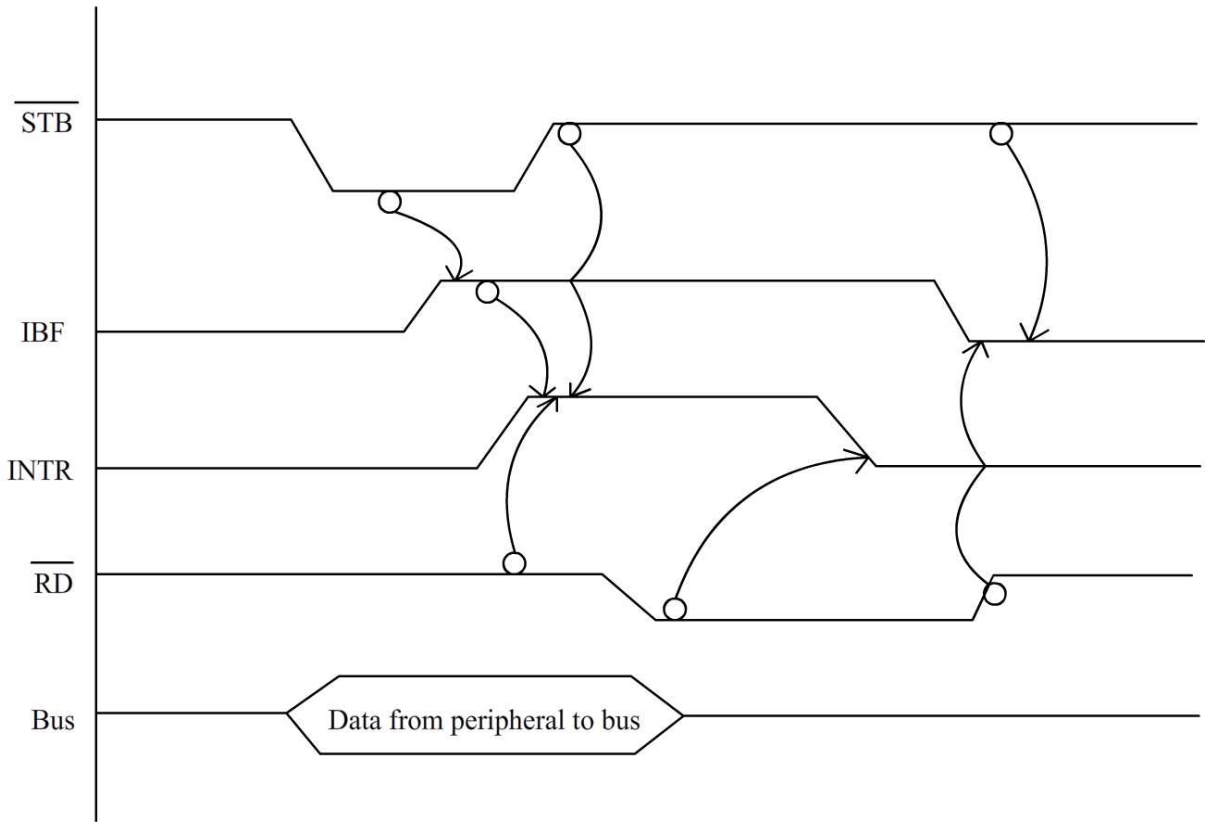
(The interrupt enable INTE f/f associated with IBF). It is controlled by bit set/reset of PC_4.

PC_3 INTRA: Interrupt request port A

A high on this output can be used to interrupt the CPU for both input output operations. When PC_6 is set, this signal indicates that the data written into port A by the CPU has been accepted by the external device. When PC_4 is set this signal indicates that the data has been written into PORT A by an external device. By proper control of PC_4&PC_6 bits an interrupt driven bidirectional 8-bit data bus between the CPU& a peripheral device or even another CPU can be established.

The timing diagram is shown below:





Special mode combination consideration:

There are several combinations of modes when not all of the bits in port C are used foe control as status. The remaining bits can be used as follows:

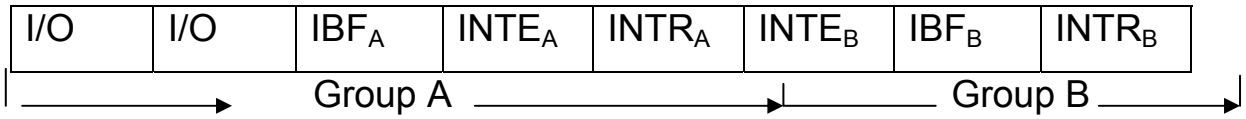
If programmed as inputs. All the input lines can be accessed during a normal PORT C read. If programmed as outputs. Bits is upper (PC3-PC0) must be individually accessed using the bit set/reset function. Bits in a lower (PC3-PC0) can be accessed using the bit set/reset function or accessed as a three some by writing into PORT C.

Reading PORT C status:

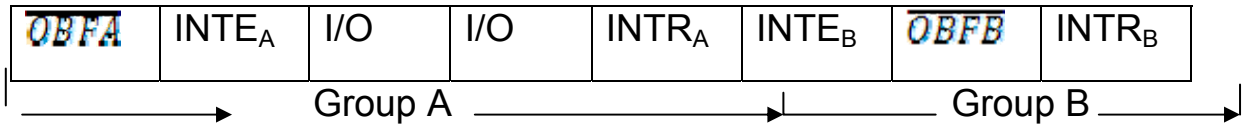
In mode '0' port C transfers data to or from the peripheral device. When the 8255 is programmed to function in mode 1 or 2, ports C generates or accept handshaking signals with the peripheral device. Reading the contents of PORT C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly. There is no special instruction to read the status information from port C. A normal read operation of PORT C is executed to perform this function.

Mode 1 Status word

Input configuration



Output configuration



Mode 2 Status word